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Claims

What is claimed is:

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1. A method for programming field programmable gate arrays (FPGA) with configuration data according to a schema developed by a developing a tool on a computer device, the method comprising by the steps of:

(a) reading said schema by a device driver from a storage device of said computer device;

(b) programming said schema by aid of a dedicated function implemented in said FPGA into an electrical erasable programmable read only memory (EEPROM) connected with said FPGA via a multiplexer, hereinafter referred to as a MUX element;

(c) switching said MUX element in order to be able to read from said EEPROM into said FPGA and

(d) triggering the configuration of said FPGA by feeding said schema from said EEPROM to said FPGA.

2. A method for using field programmable gate arrays (FPGAs) with configuration data stored in an electrical erasable programmable read only memory (EEPROM)

connected to said FPGA via a multiplexer, hereinafter referred to as a MUX element, the method comprising the steps of:

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(a) controlling said MUX element in order to be able to read from said EEPROM into said FPGA; and

(b) triggering the configuration of said FPGA by feeding said schema from said EEPROM to said FPGA.

3. A hardware circuit arrangement having a programmable read only memory (PROM) device, an electrical erasable programmable read only memory (EEPROM) device, a field programmable grate array (FPGA) device accessible via a computer bus system and a multiplexer, hereinafter referred to as a MUX element, connected between said devices, said circuit arrangement comprising:

(a) said PROM device being arranged for comprising control data for proper recognition of said FPGA by said bus system, and a logic usable for programming said EEPROM device with an EEPROM-FPGA interface;

(b) said MUX element being controllable to select either said PROM device or said EEPROM device or said FPGA device for reading data from said devices, in order to

properly connect said FPGA to said bus system and to initialize a configuration of said FPGA with contents comprised of said EEPROM.

4. The circuit arrangement according to claim 3, wherein a PC-card is detectable by a PC system bus.